ESD Testing of an EEPROM-Based Multichip Module

Harry C. Shaw, NASA/GSFC Component Technologies & Radiation Effects Branch, Code 562

Alexander A. Teverovsky, Unisys

Jeff Banker, Pico Systems Inc.

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Introduction

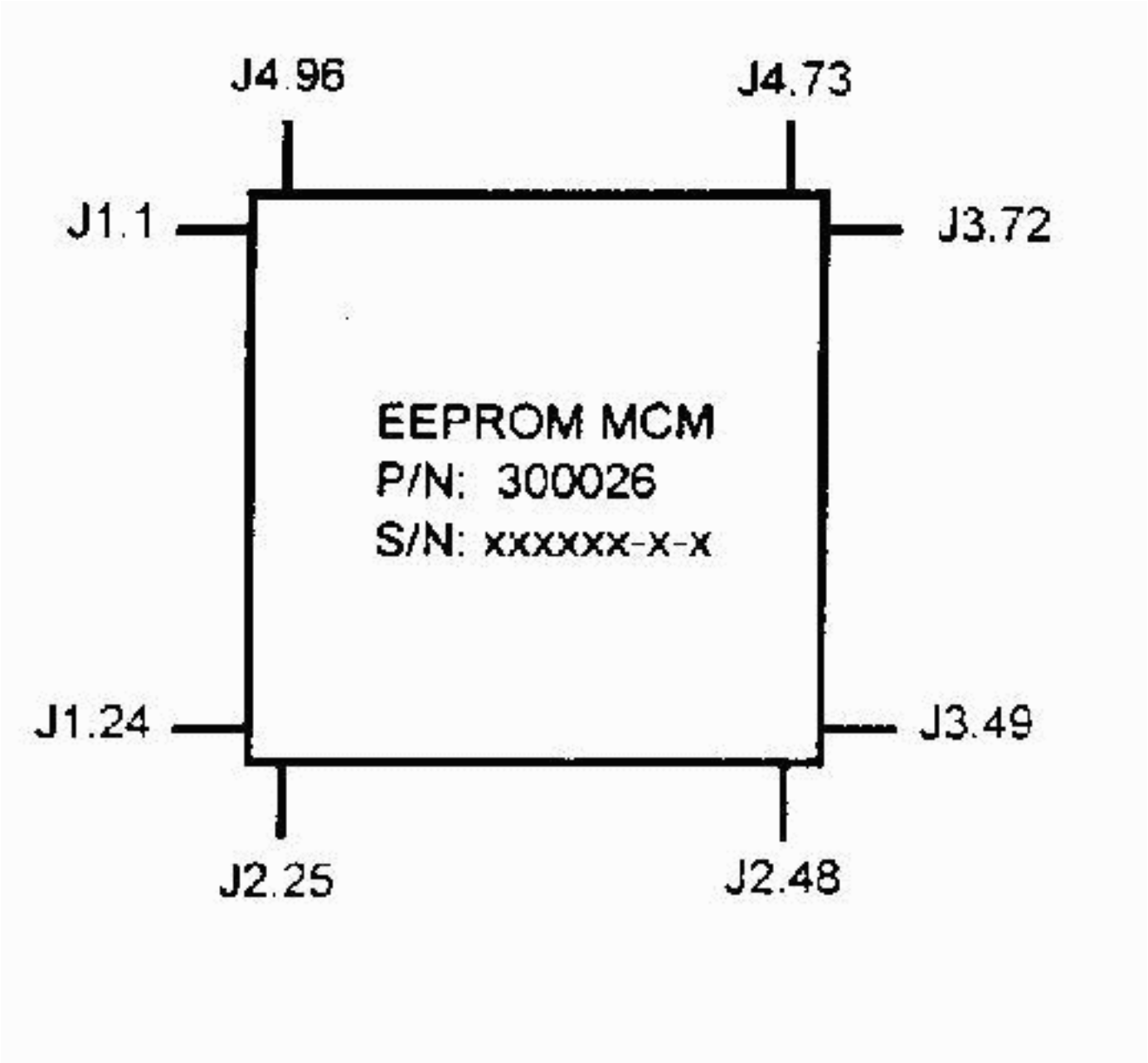
A specific multichip module (MCM) design created by Pico Systems, Inc. was tested for its sensitivity to Electrostatic Discharge or *ESD*. Testing was performed at NASA/GSFC contractor facilities in Lanham, MD during December 1997. Previously, units of this design had experienced ESD damage at the facilities of a screening subcontractor of Pico Systems Inc. The purpose of this testing was to verify the ESD sensitivity level of the MCM device and assign it a classification level according to military specifications.

This report summarizes the testing performed and the results achieved. Units remaining from a production lot for a Lockheed-Martin program were the units subjected to testing. Ultimately, the MCM device was proven to be a Class II device per MIL-STD-1686C (Human Body Model or HBM).

The MCM Circuit

The MCM circuit was composed of eight Hitachi HN58C1001 EEPROMs and three UTMC UT54ACT244 uni-directional buffer chips (see attachment to this document showing the CAD tool layout of these 11 devices). Pico Systems' programmable MCM substrate was used to provide the electrical interconnect between the chips. The substrate assembly was integrated into a 96 pin Kovar quad flat-pack. Figure 1 below defines the J1-J4 sides, which are later referred to in this document.

Figure 1: Defining Package Sides/Pins



Testing & Summary Data

ESD simulation (HBM) was performed using a manual ESD tester (ORYX, model 700). Before and after each simulation, the capacitance, C, AC conductance, G, and I-V curve (or DC resistance, R) of the corresponding pin were measured (between the pin and VCC+GND). *A 10% change in either C or G was used as the measure for determining "Failure" due to ESD damage.* A Hewlett Packard LCR meter (model 4272A) was used to get C and G readings. DC resistance and I-V curve were measured using a Tektronix curve tracer (model 370A).

The three MCM units tested consisted of serial numbers SN-4305B1-56-51 (#1), SN-4309A0 (#2), and SN-4310B0-50-48 (#3).

Unit #1

First, unit #1 was used to obtain an initial indication of the ESD susceptibility of the MCM device. During the ESD simulation, pins 48, 55, and 72 of the MCM were stressed with three positive pulses

between a pin and VCC connected to GND. If the pin did not fail, the Vzap voltage was increased with a modest increment in the range of a few hundred volts. Then, the test was repeated at the next higher voltage step. A summary table is provided below.

Table 1: Initial ESD Testing - Unit #1

Pin #	Last Good Test Voltage	Voltage @ Damage
48	3,500 V	4,000 V
55	4,500 V	5,000 V
72	7,000 V	8,000 V

Unit #2

Having established an approximate range where ESD damage starts to occur (thousands of volts), more specific testing was performed with unit #2. Minimum and maximum failing voltages were sought in order to understand the operating envelope of the device, in regards to ESD sensitivity. Since different integrated circuit devices were used at varying points in the substrate, a range of results was expected. This result is borne out in both Tables 1 and 2.

Table 2: Detailed ESD Testing - Unit #2

Data Item	Voltage Level	Pin # (If Applic.)
Minimum Failing + Voltage	4,000	50
Maximum Failing + Voltage	9,500	3
Average Failing + Voltage	6,600	N/A
Minimum Failing - Voltage	-5,500	34
Maximum Failing - Voltage	-11,000	82
Average Failing - Voltage	-8.25	N/A

The minimum failing voltage on this device was found to be +4,000 volts. Since it fails at 4,000 volts but survived at the previous voltage level of testing (3,800 V), this device is hereby classified as a Class II device according to military standards (2,000 - 3,999). Class I devices are most sensitive (0-1,999 volts survivability). It should also be noted that most of the failures occurred with positive voltage with only a

few occurring with a negative pulse of ESD.

Unit #3

Unit #3 was tested in a manner similar to MIL-STD-883, Test Method 3015 requirements. For this purpose, pins on the sides J1 and J4 were stressed relatively to GND (all other pins open), pins on the side J2 were stressed relative to VCC (all others open), and pins on the side J3 were stressed to all others connected (except VCC and GND).

Three pulses of each voltage magnitude in the following sequence were applied: -2,000V, +2,000V, -4,000 V, and +4,000 V. Parameters were measured before testing the side, and before and after each pin testing. Testing at +/- 2,000 V is used to mimic Direct Contact of Non-Operating Assembly. Testing at +/- 4,000 V is used to mimic Director Contact of Operating Equipment per the MIL-STD.

Table 3: Detailed ESD Testing - Unit #3

Data Item	Voltage Level	Pin # (If Applic.)
Side J1 Min. Failing + Voltage	4,000	23
Side J1 Min. Failing - Voltage	4,000	24
Side J2 Min. Failing + Voltage	4,000	30,31,35,36
Side J2 Min. Failing - Voltage	4,000	25,48
Side J3 Min. Failing + Voltage	4,000	54
Side J3 Min. Failing - Voltage	4,000	49,50,66,70-72
Side J4 Min. Failing + Voltage	4,000	78
Side J4 Min. Failing - Voltage	4,000	96

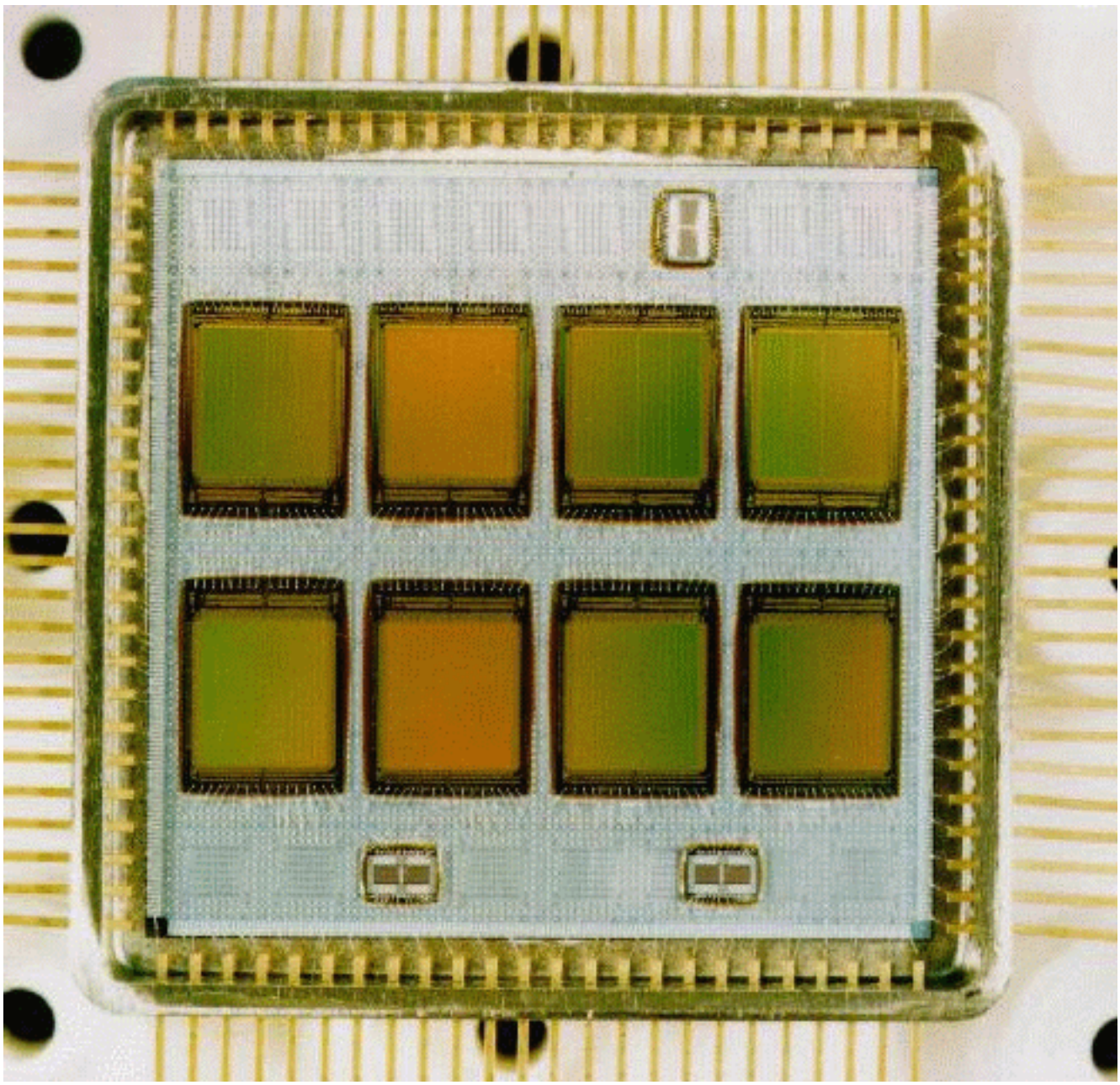
All of the tested pins passed three pulses at each magnitude of +/- 2,000 volts, which agrees with unit #2 (Class II device). The pins noted in this table above are only those that "failed" after being subjected to three ESD pulses of magnitude +/- 4,000 volts. It is suspected that the actual failures would have occurred close to 4,000 volts, similar to device #2. However, military specifications for ESD testing only specify the three pulses at +/- 2,000 volts and then +/- 4,000 volts. This testing is sufficient to classify the device as Class I (0-1,999V), II (2,000-3,999V), or III (4,000V & up) in regards to ESD susceptibility to the Human Body Model.

Summary & Conclusion

The ESD tolerance of the EEPROM MCM manufactured by Pico Systems was fond to correspond to the Class II grouping of military standards (2,000 - 3,999 V) for the HBM. Polarity of the voltage, quantity

of pulses, and type of the signal did not affect the ESD susceptibility with any significance.

Note: Here's a picture of the part:



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